**Lab 11**

**A Taste of Data path + Control Design Example:**

**Factorial Circuit (Open Ended Lab)**



**Spring 2025**

Submitted by: **Mohsin Sajjad**

Registration No: **22pwsce2149**

Class Section: **A**

“On my honor, as student of University of Engineering and Technology, I have neither given nor received unauthorized assistance on this academic work.”



Student Signature: \_\_\_\_\_\_\_\_\_\_\_\_\_\_

Submitted to:

**Engr. Faheem Jan**

Month Day, Year (22 05, 2025)

Department of Computer Systems Engineering

University of Engineering and Technology, Peshawar

**A Taste of Data path + Control Design Example:**

**Factorial Circuit (Open Ended Lab)**

**Objective:**

To implement a circuit that calculates factorial of a number.

**Block Diagram:**

The datapath for calculating the factorial of an “N” bit number is

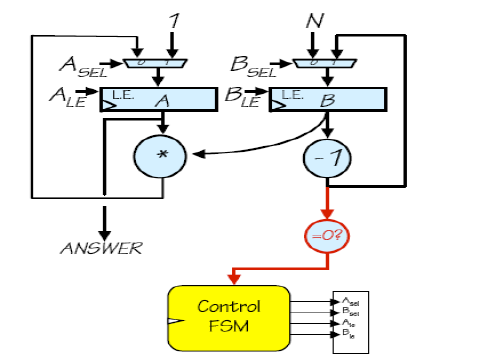
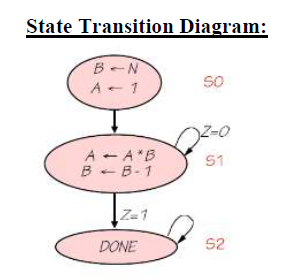
given below. The datapath is controlled by a Finite State Machine (FSM). FSM

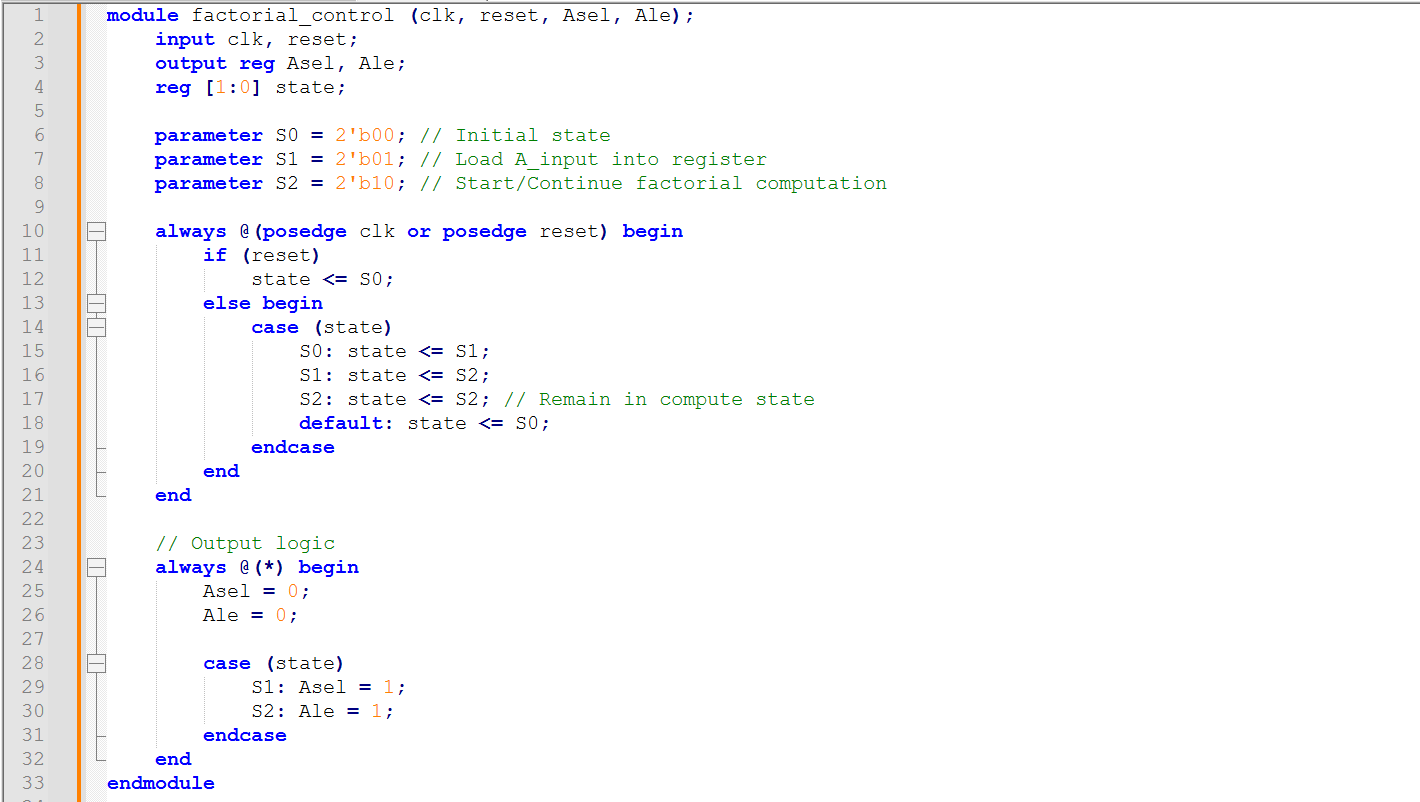
generates signals Asel, Ale, Bsel and Ble at the correct times to operate the

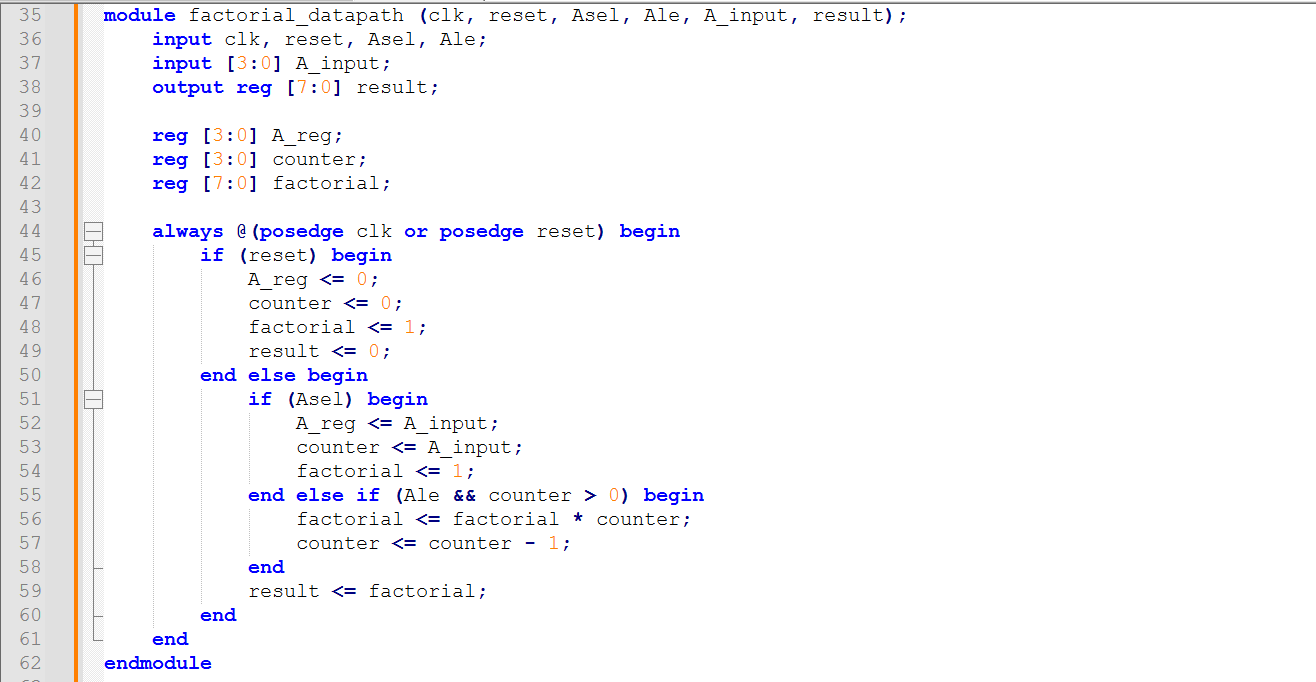
datapath. Input to FSM is a signal “Z” when Z=0 means the operation of the

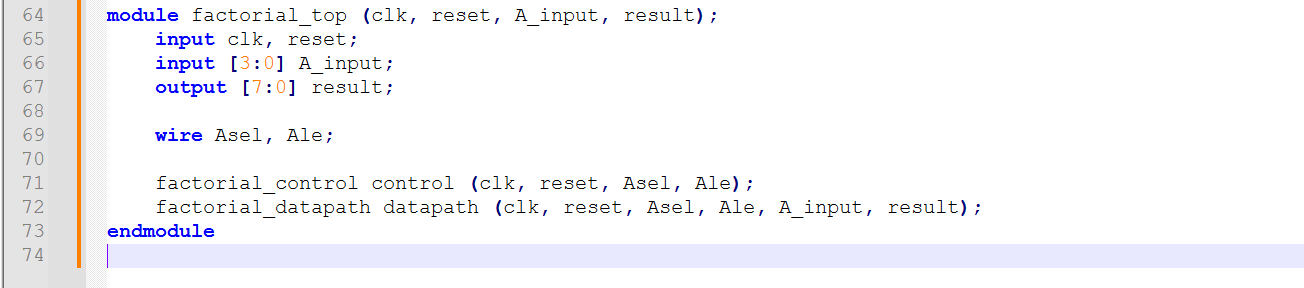
machine is complete and ANSWER can be read. The STG is also given in the

following diagram.

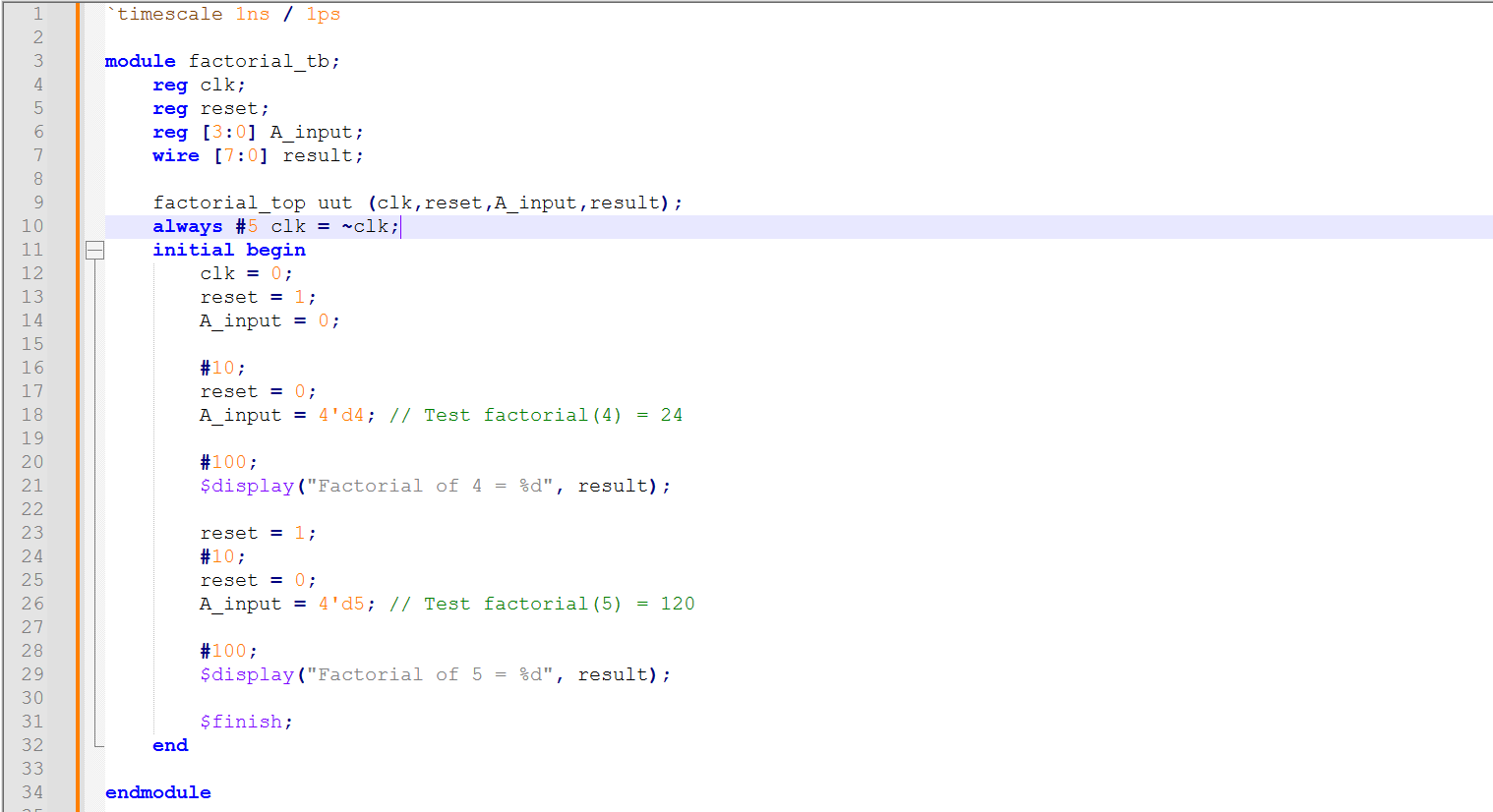
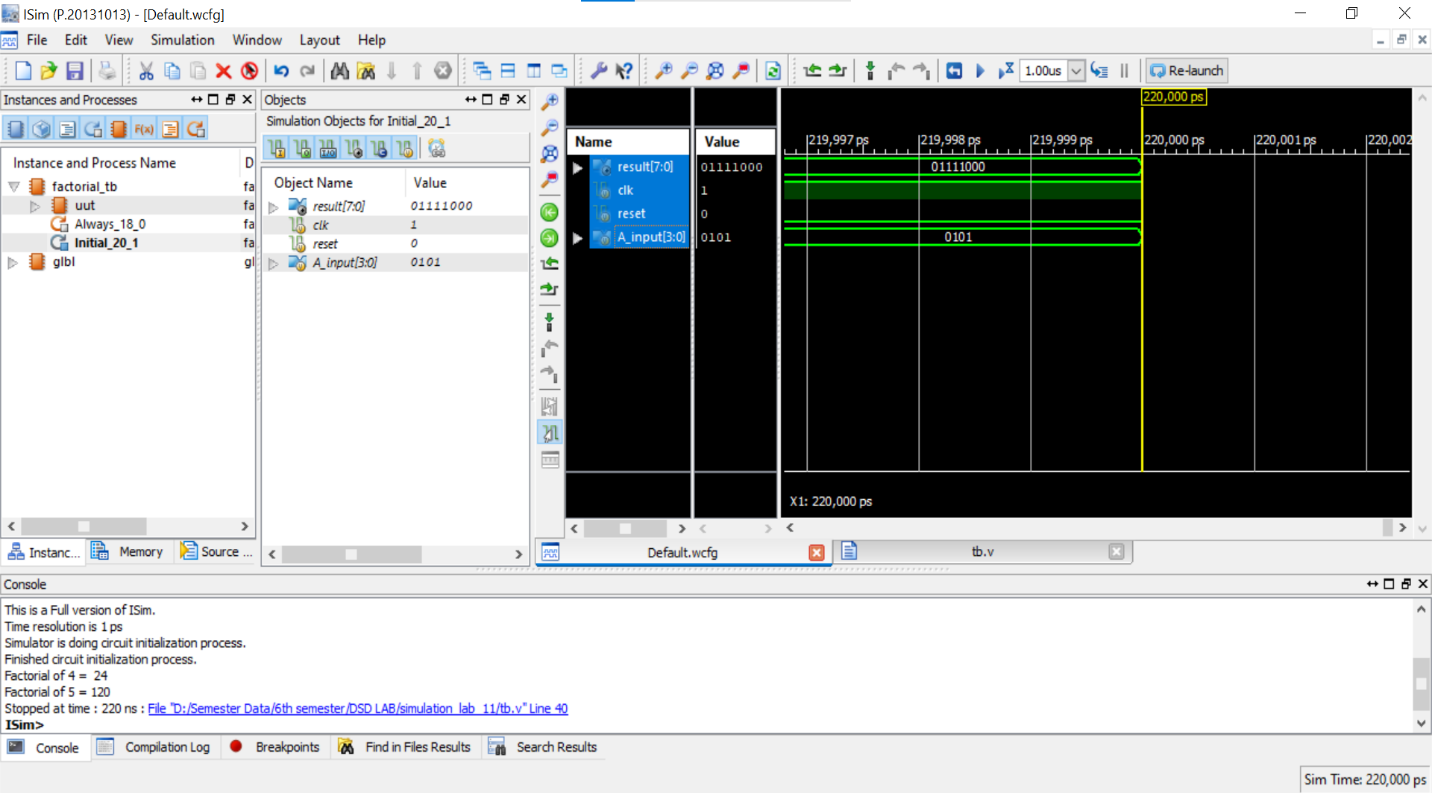


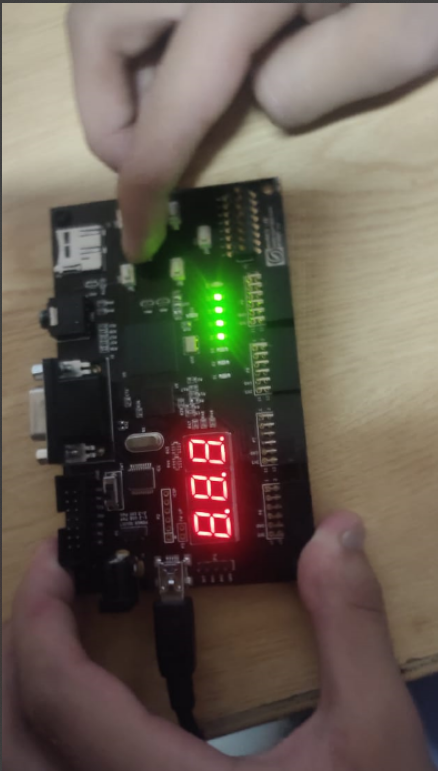
**CODE:**  






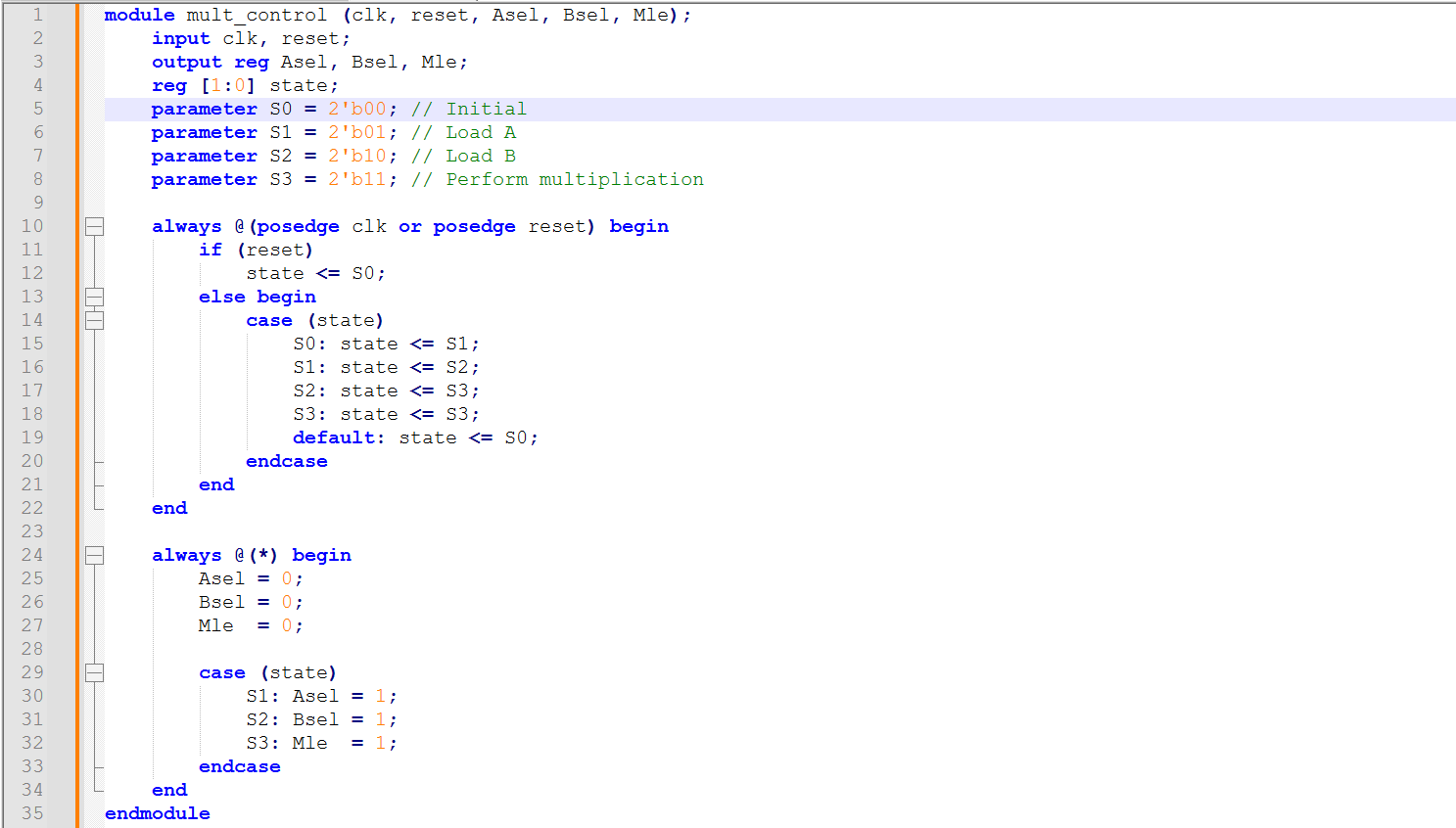
Test-Bench:

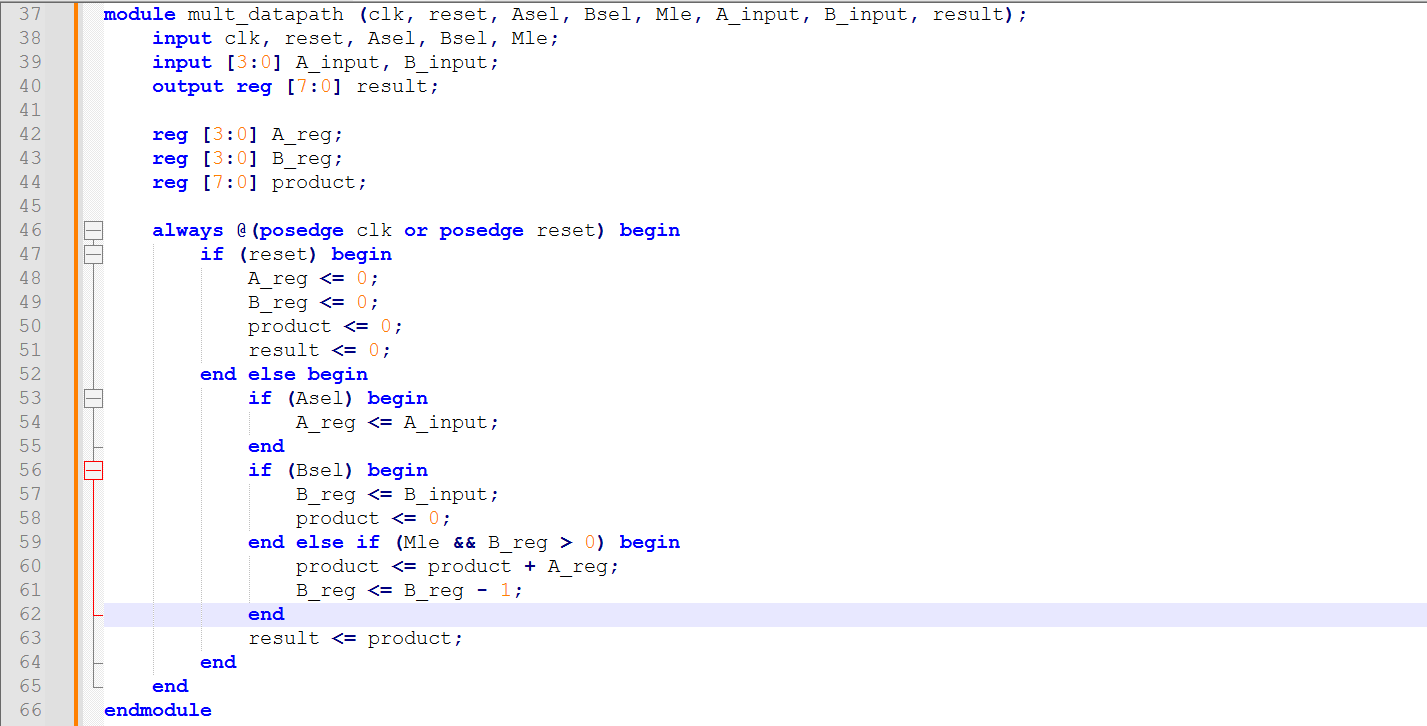
**OUTPUT:**  


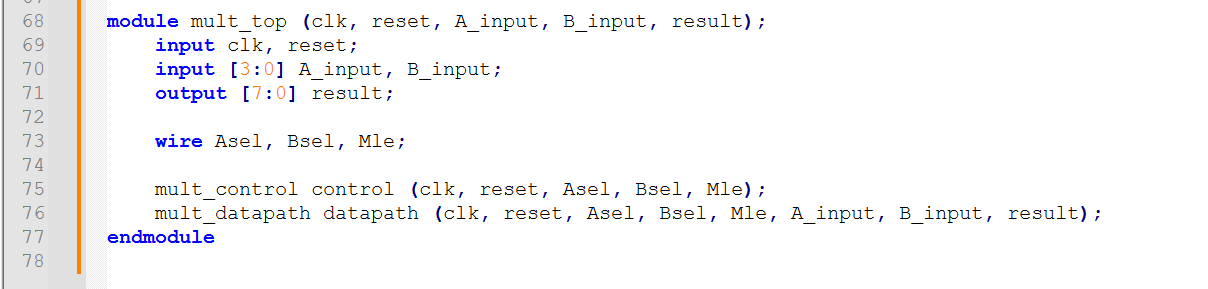
**Output on FPGA:  
**

**Task 2:** Implement Multiplication for repeated addition using data path and control path (FSM)

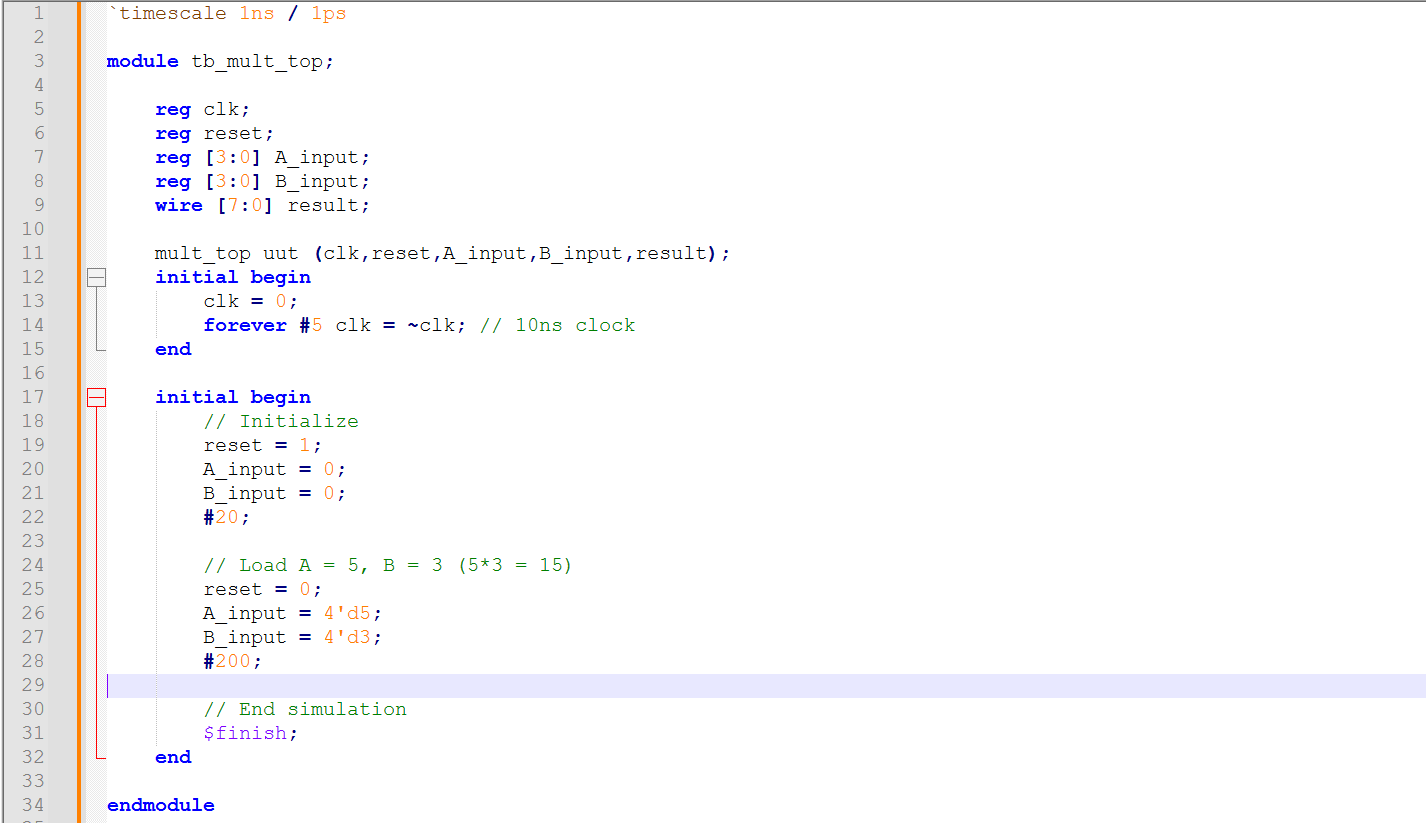
Note: you can do simulation as well

**CODE:  
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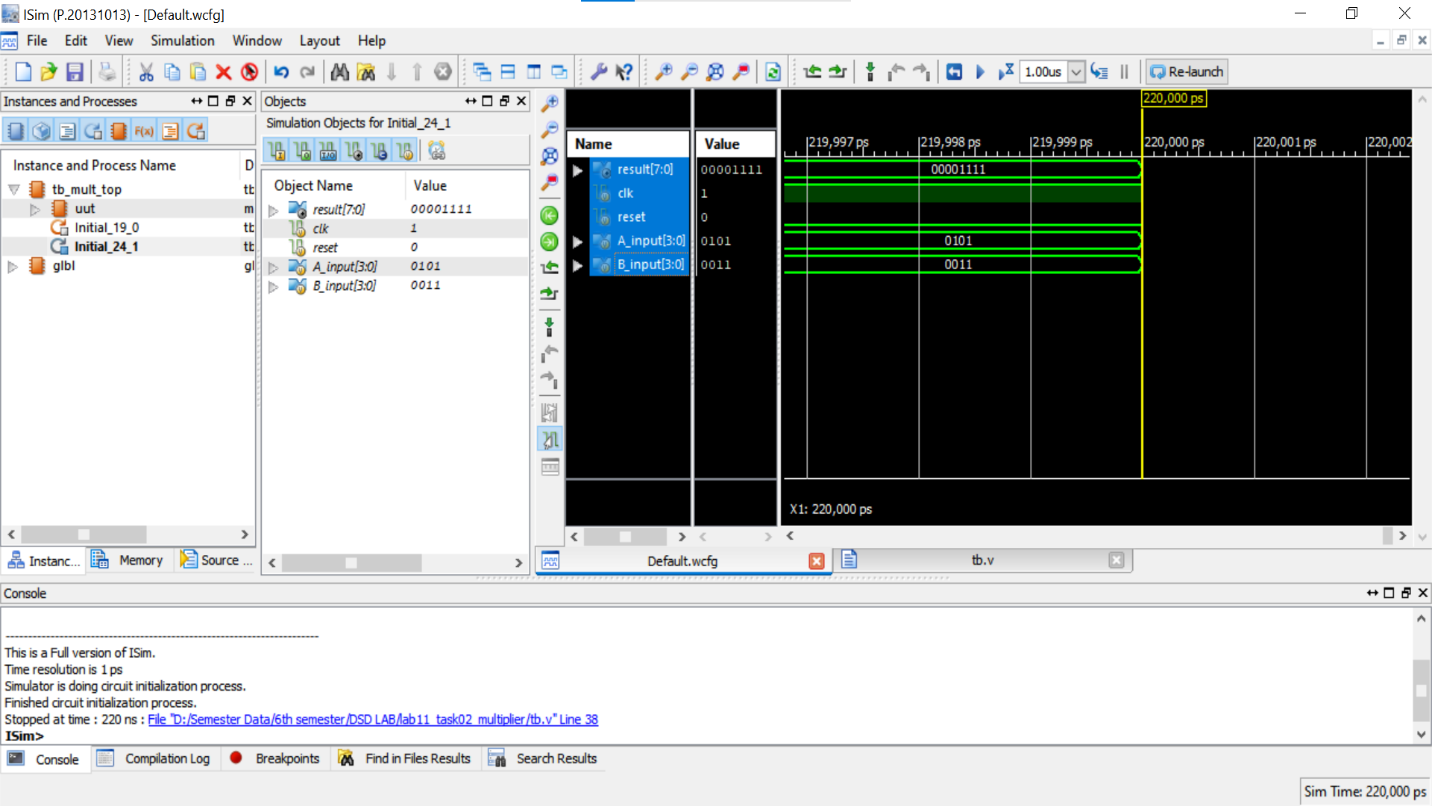
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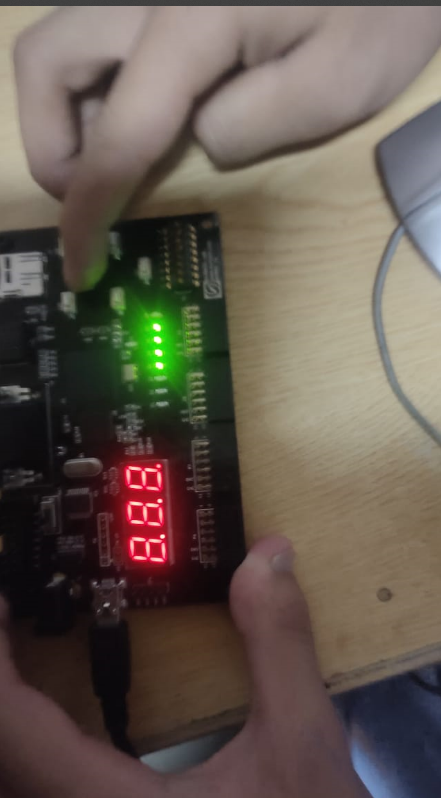
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**Test-Bench:**



**OUTPUT:**

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